CLAIMS

What is claimed is:

1. A method of measuring signal skew of a signal tree on a programmable logic device, the signal tree having a source node connected to first and second destination branches, a first plurality of programmable logic blocks programmably connectable to the first destination branch, and a second plurality of programmable logic blocks programmably connectable to the second destination branch, each of the logic blocks having an input terminal and an output terminal, the method comprising:
   a. instantiating a first oscillator on the device using a first programming sequence that includes:
      i. connecting the first destination branch to the input terminal of one of the first plurality of logic blocks;
      ii. connecting the output terminal of the one of the first plurality of logic blocks to the input terminal of one of the second plurality of logic blocks; and
      iii. connecting the output terminal of the one of the second plurality of logic blocks to the source node;
   b. measuring the period the first oscillator; and
   c. instantiating a second oscillator on the device using a second programming sequence that includes:

i. connecting the second destination branch to the input terminal of one of the second plurality of logic blocks;

ii. connecting the output terminal of the one of the second plurality of logic blocks to the input terminal of a second one of the second plurality of logic blocks; and

iii. connecting the output terminal of the second one of the second plurality of logic blocks to the source node; and

d. measuring the period of the second oscillator.

2. The method of claim 1, wherein the one of the second plurality of logic blocks in the first oscillator and the second one of the second plurality of logic block in the second oscillator are the same logic block.

3. The method of claim 1, further comprising:

e. instantiating a third oscillator on the device using a third programming sequence that includes:

i. connecting the first destination branch to the input terminal of a first of the first plurality of logic blocks;

ii. connecting the output terminal of the first of the first plurality of logic blocks to the input terminal of a second of the first plurality of logic blocks; and

iii. connecting the output terminal of the second of the first plurality of logic blocks to the source node; and

f. measuring the period the third oscillator.

4. The method of claim 3, wherein the second of the first plurality of logic blocks is the one of the first plurality of logic blocks one of the second plurality of logic blocks of paragraph (1)(a).

5. The method of claim 4, further comprising:
   g. instantiating a fourth oscillator on the device using a fourth programming sequence that includes:
      i. connecting the second destination branch to the input terminal of one of the first plurality of logic blocks;
      ii. connecting the output terminal of the one of the second plurality of logic blocks to the input terminal of one of the first plurality of logic blocks;
      iii. connecting the output terminal of the one of the first plurality of logic blocks to the source node;
   h. measuring the period the fourth oscillator.

6. The method of claim 5, wherein the one of the first plurality of logic blocks is the same one of the first plurality of logic blocks of paragraph (1)(a).

7. The method of claim 6, wherein the one of the second plurality of logic blocks is the same one of second plurality of logic blocks of paragraph (1)(a).

8. The method of claim 3, further comprising:

g. instantiating a fourth oscillator on the device using a fourth programming sequence that includes:

i. connecting the first destination branch to the input terminal of a third of the first plurality of logic blocks;

ii. connecting the output terminal of the third of the first plurality of logic blocks to the input terminal of the first the first plurality of logic blocks; and

iii. connecting the output terminal of the first of the first plurality of logic blocks to the source node.

9. A method of measuring signal skew of a signal tree on a programmable logic device, the signal tree having a source node connected to first and second destination branches, a first plurality of programmable logic blocks programmably connectable to the first destination branch, and a second plurality of programmable logic blocks programmably connectable to the second destination branch, each of the logic blocks having an input terminal and an output terminal, the method comprising:

a. instantiating a first oscillator on the device using a first programming sequence that includes:

i. connecting the first destination branch to the input terminal of a first of the first plurality of logic blocks;

ii. connecting the output terminal of the first logic block to the input terminal of a

second one of the first plurality of logic blocks;

iii. connecting the output terminal of the second logic block to the source node; and

b. instantiating a second oscillator on the device using a second programming sequence that includes:

i. connecting the first destination branch to the input terminal of the second logic block;

ii. connecting the output terminal of the second logic block to the input terminal of a first logic block;

iii. connecting the output terminal of the first logic block to the source node.

10. A method comprising:

a. programming a programmable logic device to include a first delay element, the first delay element including:

i. a first destination branch connected to a source node;

ii. a first logic block having a first input terminal and a first output terminal, wherein the first input terminal is programmably connected to the first destination branch;

iii. a second logic block having a second input terminal and a second output terminal, wherein the second terminal is programmably connected to the first output terminal; and

b. programming the programmable logic device to include a second delay element, the second delay element comprising:

   i. the first logic block, wherein the first input terminal is programmably connected to the second output terminal;

   ii. the second logic block, wherein the second terminal is programmably connected to the first destination branch.

11. A method of measuring skew on a programmable logic device, the device including a distribution network having a source node connected to a destination branch and a plurality of programmable logic blocks programmably connectable to the destination branch, each of the logic blocks having an input terminal and an output terminal, the method comprising the steps of:

a. instantiating a first delay element on the device using a first programming sequence that includes:

   i. connecting the destination branch to the input terminal of a first of the plurality of logic blocks;

   ii. connecting the output terminal of the first of the plurality of logic blocks to the input terminal of a second of the plurality of logic blocks; and

b. instantiating a second delay element on the device using a second programming sequence that includes:

i. connecting the destination branch to the input terminal of a third of the plurality of logic blocks;

ii. connecting the output terminal of the third of the plurality of logic blocks to the input terminal of the second of the plurality of logic blocks; and

c. comparing the signal propagation delays through the first and second delay elements.

12. The method of claim 11, wherein the first delay element is part of a first ring oscillator and the second delay element is part of a second ring oscillator, and wherein the respective signal propagation delays through the first and second delay elements are proportional to the respective periods of the first and second oscillators.

13. The method of claim 11, wherein the programmable logic device further includes a second destination branch connected to the source node and a second plurality of programmable logic blocks programmably connectable to the second destination branch, each of the logic blocks having an input terminal and an output terminal, the method further comprising the steps of:

d. instantiating a third delay element on the device using a third programming sequence that includes:

i. connecting the second destination branch to the input terminal of a first of the second plurality of logic blocks; and

ii. connecting the output terminal of the first of the second plurality of logic blocks to

the input terminal of a second of the second plurality of logic blocks; and

e. instantiating a fourth delay element on the device using a fourth programming sequence that includes:

i. connecting the second destination branch to the input terminal of a third of the second plurality of logic blocks;

ii. connecting the output terminal of the third of the second plurality of logic blocks to the input terminal of the second of the second plurality of logic blocks.

14. The method of claim 13, wherein the first delay element is part of a first ring oscillator, the second delay element is part of a second ring oscillator, the third delay element is part of a third ring oscillator, and the fourth delay element is part of a fourth ring oscillator, and wherein the respective signal propagation delays through the first, second, third, and fourth delay elements are proportional to the respective periods of the first, second, third, and fourth oscillators.

15. The method of claim 11, wherein the second logic block is adjacent the first and third logic blocks on the programmable logic device.

16. A method of calculating a first signal propagation delay along a portion of a signal distribution network on a programmable logic device, the method comprising:

a. instantiating a first delay element on the device using a first programming sequence, wherein the first delay element includes the portion of the signal distribution network;

b. determining a second signal propagation delay through the first delay element;

c. instantiating a second delay element on the device using a second programming sequence, wherein the second delay element includes the portion of the signal distribution network; and

d. determining a third signal propagation delay through the second delay element.

17. The method of claim 16, wherein the first signal propagation delay is proportional to the difference between the second and third signal propagation delays.

18. The method of claim 16, wherein instantiating the first delay element includes instantiating a first ring oscillator that includes the first delay element, and wherein instantiating the second delay element includes instantiating a second ring oscillator that includes the second delay element.

19. The method of claim 18, wherein determining the second and third signal propagation delays includes measuring the oscillation period of the respective first and second oscillators.